1. (Currently Amended) A device, comprising:

a plurality of ~~one or more~~ active substrates comprising substantially transistors or diodes formed thereon;

one or more passive substrates comprising substantially inductors, capacitors or resistors formed thereon;

a plurality of bonding pads positioned on the active and passive substrates including intra-substrate pads adapted to support wire-bonding within a substrate; and

bonding wires connected to the bonding pads.

2. (Original) The device of claim 1, further comprising a die pad to receive the active and passive substrates.

3. (Original) The device of claim 2, further comprising one or more pins and wherein one or more of the bonding wires connect one or more bonding pads to the one or more pins.

4. (Currently Amended) The device of claim 1, wherein the active and passive substrates comprise gallium arsenide substrates.

5. (Original) The device of claim 1, wherein the active substrate comprises supporting passive components.

6. (Currently Amended) The device of claim 1, further comprising a ~~substantially~~ passive IC coupled to the active substrate.

7. (Original) The device of claim 1, further comprising one or more substantially passive ICs for passive components only.

8. (Currently Amended) The device of claim 1, wherein the active and passive substrates are interconnected with bonding wires.

9. (Currently Amended) The device of claim 1, wherein the active and passive substrates are mounted on a metal die pad.

10. (Currently Amended) The device of claim 1, wherein the active and passive substrates are encapsulated in molded plastics or other insulating medium.

11. (Original) The device of claim 1, wherein the active substrates comprises primarily transistors.

12. (Currently Amended) The device of claim 11, wherein the transistors include silicon bipolar, CMOS, RFCMOS, ~~BICOMS~~ BiCMOS, SiGe, GaAs HBT, or HEMT.

13. (Original) The device of claim 11, wherein the transistors are fabricated on a wafer with semiconductor layer structure, junctions, and dopings.

14. (Original) The device of claim 1, wherein the passive substrate comprises a network of resistor (R), inductor (L), and capacitor (C) without active device structure.

15. (Original) The device of claim 1, wherein the passive substrate comprises one or more conductive metal layers for inductor (L) and interconnection.

16. (Original) The device of claim 1, wherein the passive substrate comprises an insulating layer with suitable dielectric properties.

17. (Original) The device of claim 16, wherein the insulating layer comprises Nitride or Oxide as the dielectric layer for a capacitor (C).

18. (Original) The device of claim 1, wherein the passive substrate comprises a layer including TaN or NiCr for a resistor (R).

19. (Original) The device of claim 1, wherein the passive substrate comprises one or more circuits of passive components including transmission lines, impedance matching network, filters, baluns, or diplexers.

20. (Original) The device of claim 1, wherein the passive substrate is fabricated using fewer fabrication steps than the active substrate.